# Derandomizing Polynomial Identity Tests Means Proving Circuit Lower Bounds

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# Contents

#### Introduction

Preliminaries

Lemma 1

Lemma 2

Lemma 3

Proof of Theorem

Conclusion

**Open Problems** 

References

# 

# Introduction

- We present a summarized interpretation of the paper Derandomizing Polynomial Identity Tests Means Proving Circuit Lower Bounds [KI03] by Valentine Kabanets and Russell Impagliazzo, based on our reading of the paper.
- Following is the main theorem of the paper

# Theorem

 $PIT \in P \implies per \notin Arth - P/poly \text{ or } NEXP \nsubseteq P/poly$ 



# Structure

- Preliminaries: Arithmetic circuits, PIT, PRGs
- Lemma 1  $PIT \in P$  and  $per \in Arth - P/poly \implies P^{per} \subseteq NP$ .
- Lemma 2  $EXP \subseteq P/poly \implies EXP = MA$
- Lemma 3  $NEXP \in P/poly \implies NEXP = EXP$ .
- Proof of Theorem: Combining to get the main theorem.
- Conclusion: Implications and Future Scope

# IntroductionPreliminariesLemma 1Lemma 2Lemma 3Proof of TheoremConclusionOpen ProblemsReferences000000000000000000000

# Arithmetic circuits

- Representation for polynomials
- A Directed Acyclic Graph that computes a polynomial f over  $\mathbb{F}$  and set of variables  $x_1, \ldots, x_n$
- Vertices of in-degree 0 labeled with variable or field element
- All other vertices(gates) labeled with + or imes
- Edges labeled with field constants (1 by default)
- Size: number of edges
- For more details on Arithmetic circuits, check [SY10]



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# Polynomial Identity Testing(PIT)

- Efficiently test whether an input polynomial as circuit is identically zero or not.
- For univariate, just check at *degree* + 1 points. Doesn't work for multivariate.
- For more details on PIT, check [Sax09]

# IntroductionPreliminariesLemma 1Lemma 2Lemma 3Proof of TheoremConclusionOpen ProblemsReferences000000000000000000000

# **Randomized Solution**

#### Lemma

**(PIT Lemma)**(Schwartz-Zippel[Sch80]) Let  $f \in \mathbb{F}[x_1, \ldots, x_n]$  be a non-zero polynomial of total degree  $d \ge 0$ . Let S be any finite subset of  $\mathbb{F}$ , and let  $\alpha_1, \ldots, \alpha_n$  be elements selected independently, uniformly and randomly from S. Then,

$$Pr_{\alpha_1,\ldots,\alpha_n\in S}[f(\alpha_1,\ldots,\alpha_n)=0]\leq \frac{d}{|S|}$$

# IntroductionPreliminariesLemma 1Lemma 2Lemma 3Proof of TheoremConclusionOpen ProblemsReferences00000000000000000000

# **Randomized Solution**

#### Lemma

**(PIT Lemma)**(Schwartz-Zippel[Sch80]) Let  $f \in \mathbb{F}[x_1, \ldots, x_n]$  be a non-zero polynomial of total degree  $d \ge 0$ . Let S be any finite subset of  $\mathbb{F}$ , and let  $\alpha_1, \ldots, \alpha_n$  be elements selected independently, uniformly and randomly from S. Then,

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- Thus  $PIT \in coRP$
- Open: Derandomizing PIT in poly(s)-time



# Pseudorandomness Generators(PRGs)

- Decrease the number of random bits required.
- For  $S : \mathbb{N} \to \mathbb{N}$ , a  $2^{O(n)}$ -computable function  $G : \{0,1\}^* \to \{0,1\}^*$  is an S - prg, if  $\forall I$ ,  $G : \{0,1\}^I \to \{0,1\}^{S(I)}$ , and  $\forall$  circuits C of size  $\leq S(I)^3$

$$|Pr_{x \in U_{l}}[C(G(x)) = 1] - Pr_{x \in U_{S(l)}}[C(x) = 1]| < 0.1$$

#### 

# Pseudorandomness Generators(PRGs)

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 $BP - TIME(S(I(n))) \subseteq DTIME(2^{I(n)}S(I(n)))$ 

• A  $2^{\epsilon l}$ -prg  $\implies$  BPP=P

# Introduction Preliminaries Lemma 1 Lemma 2 Lemma 3 Proof of Theorem Conclusion Open Problems References of the concept of the

• Worst-case Hardness For  $f : \{0,1\}^* \to \{0,1\}, H_{wrs}(f)$  is the largest S(n) st.  $\forall$  circuit  $C_n \in size(S(n))$ ,

$$Pr_{x\in U_n}[C_n(x)=f(x)]<1$$

Average-case Hardness H<sub>avg</sub>(f) is the largest S(n) st. ∀ circuit C<sub>n</sub> ∈ size(S(n)),

$$Pr_{x \in U_n}[C_n(x) = f(x)] < \frac{1}{2} + \frac{1}{S(n)}$$

• Can be shown that a worst-case hard function gives also an average-case hard function.



**NW-Design** 

Theorem If  $\exists f \in E$  with  $H_{avg} \geq S(n)$ , then  $\exists S'(l)$ -prg, where  $S'(l) = S(n)^{0.01}$ .



#### Lemma

# $PIT \in P \text{ and } per \in Arth - P/poly \implies P^{per} \subseteq NP.$

#### **Proof Idea**

- "Guess" the small circuit for permanent and verify it using  $PIT \in P$ .
- per<sub>n</sub>(A) = ∑<sub>i∈[n]</sub> A<sub>1i</sub>.per(A'<sub>1i</sub>) where A'<sub>1i</sub> is the corresponding minor.

Introduction	Preliminaries	Lemma 1	Lemma 2	Lemma 3	Proof of Theorem	Conclusion	Open Problems	References
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- Let *C<sub>n</sub>* be arithmetic circuit corresponding to the *per<sub>n</sub>*.
- Protocol for obtaining the circuit.
  - 1. Given  $C_{n-1}$ , we guess the circuit for  $C_n$  as follows:

$$C_n(A) = \sum_{i \in [n]} A_{1i}.C_{n-1}(A'_{1i})....(1)$$

- 2. Use PIT for verifying whether the above expression is correct or not.
- 3. Repeat it for circuits  $C_{n-1}$  which we used for minors and so on.
- Using this recursive guess and verify procedure, we can get a circuit  $C_n(A) = per_n(A)$  by induction on n.

Introduction	Preliminaries	Lemma 1	Lemma 2	Lemma 3	Proof of Theorem	Conclusion	Open Problems	References
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- Now we show  $P^{per} \subseteq NP$
- Let  $L \in P^{per}$ .

Guess  $C_n$  for  $per_n$  using the recursive procedure. Use this circuit  $C_n$  for  $per_n$  instead of the oracle

- $PIT \in P$ , implies the entire verification is in P.
- per ∈ Arth − P/poly, implies the guess that our machine need to do is poly-sized.
- This gives  $L \in NP \implies P^{per} \subseteq NP$



#### Lemma

 $EXP \subseteq P/poly \implies EXP = MA$ 

**Proof Idea** First show  $EXP \subseteq P/poly \implies EXP = \Sigma_2$ .

- Consider *L* ∈ *EXP*, with TM N. Encode steps of *N* Using the circuit and ∃∀
- Compute *j*-th bit of *i*-th configuration of N(x) in exp-time
  ⇒ ∃ poly-size C(x, i, j) computing it.
- $x \in L \iff \exists C, \forall (i,j) [C(x,i,j) \rightarrow C(x,i+1,j) \text{ is a valid step }].$
- Thus,  $EXP = \Sigma_2$



#### Lemma

 $EXP \subseteq P/poly \implies EXP = MA$ 

- $\Sigma_2 \subseteq PSPACE = IP \subseteq EXP = \Sigma_2$ , i.e.  $PSPACE = IP = EXP \subseteq P/poly$ .
- We have a IP protocol for *L*. We convert it one round.
- Prover in IP is a PSPACE machine, simulate using a poly-size circuit family {C<sub>n</sub>}<sub>n∈ℕ</sub>
- 1-round protocol for checking x ∈ L:
  Prover: Send his circuit C<sub>n</sub>, for n = |x|.
  Verifier: Simulate the IP protocol using C<sub>n</sub> as P.
- Thus, EXP = MA



#### Lemma $NEXP \subseteq P/poly \implies NEXP = EXP$ **Proof Idea**

• Assume  $\exists L \in NEXP \setminus EXP$ , st.  $\exists c > 0$  and machine R(x, y) running in  $exp(|x|^{10c})$ 

$$x \in L \iff \exists y \in \{0,1\}^{exp(|x|^c)} R(x,y) = 1$$

• *y* is hard for *EXP*, we use it compute hard-function, consider function whose Truth table is *y*.



#### Lemma $NEXP \subseteq P/poly \implies NEXP = EXP$

#### Proof Idea contd.

Consider the machine  $M_D$ ,  $\forall D > 0$  as follows:

- construct tt of all circuits of size  $n^{100D}$ , with  $n^c$  input.
- if  $\exists C, R(x, tt) = 1$  ACCEPT, else REJECT

**Running Time:**  $exp(n^{100D} + n^{10c})$ 



#### Lemma

# $\textit{NEXP} \subseteq \textit{P/poly} \implies \textit{NEXP} = \textit{EXP}$

- $L \notin EXP \implies M_D$  cannot solve L
- Therefore, for infinitely many x's, y is such that  $H_{wrs}(f_y) > n^{100D}$ .
- Using NW design we have a I<sup>D</sup> prg.



Lemma  $NEXP \subseteq P/poly \implies NEXP = EXP$ 

- $EXP \subset NEXP \subseteq P/poly$ . So from lemma 2, we have an EXP=MA
- ∀L ∈ EXP, Merlin tries to show that x ∈ L by sending a short proof to Arthur.
- Arthur verifies it using a randomised algo in say  $n^D$  steps.
- Using the  $I^D$  prg, we can reduce the number of random bits from  $n^D$  to n for Arthur.



# Lemma $NEXP \subseteq P/poly \implies NEXP = EXP$

- If we have n as the input length of some string which is "hard" for the tt circuits, we can replace Arthur by a non-deterministic algorithm in  $poly(n^d)2^{n^c}$  time that does not toss any random coins by using the prg obtained before (the  $2^{n^c}$  factor is for calculating the n random bits deterministically)
- This gives  $L \in \mathsf{NTIME}(2^{n^{c'}})$  "infinitely often" with n-bit advice. Thus  $EXP \subseteq \mathsf{NTIME}(2^{n^{c'}})$  "infinitely often" with n-bit advice
- But NEXP ⊆ P/poly. Thus we have NTIME (2<sup>n<sup>c'</sup></sup>)
  ⊆ SIZE(n<sup>c'</sup>) for a constant c'. So EXP ⊆ SIZE(n<sup>c'</sup>) infinitely often (the n bit advice can be hardcoded in the circuit).



# Lemma $NEXP \subseteq P/poly \implies NEXP = EXP$

#### Proof Idea contd.

•  $\exists$  c' such that every language in EXP can be decided on infinitely many inputs by a circuit family of size  $n + n^{c'}$ . Yet this can be ruled out using elementary diagonalization (more details in the paper)

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# Proof of Theorem

#### Theorem

 $PIT \in P \implies per \notin Arth - P/poly \text{ or } NEXP \not\subseteq P/poly$ 

- Suppose PIT ∈ P, per ∈ Arth P/poly and NEXP ⊆ P/poly.
- From lemmas 2 and 3,  $NEXP = EXP = MA \subseteq PH$ .
- Also PH ⊆ P<sup>per</sup> (Toda's theorem)
- So NEXP ⊆ P<sup>per</sup>
- Now as we have PIT ∈ P and per ∈ Arth P/poly, using lemma 1, we get P<sup>per</sup> ⊆ NP
- Combining these two, we get NEXP ⊆ NP which contradicts the non-deterministic time hierarchy theorem. Thus atleast of the assumptions is false which gives:

 $PIT \in P \implies per \notin Arth - P/poly \text{ or } NEXP \nsubseteq P/poly$ 



- Derandomizing RP or BPP would give us circuit lower bounds for NEXP or for permanent.
- The results in the present paper do not rule out that ZPP = P can be proved without having to prove any circuit lower bounds first. This leaves some hope that unconditional derandomization of ZPP could be achieved.



# **Open Problems**

- BPP = P, PIT ∈ P, per ∉ Arth P/poly and NEXP ⊈ P/poly.(we believe all of these to be true)
- Does BPP=P imply circuit lower bounds for EXP (instead of NEXP) ?





# Questions ?



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